AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

Claim 1 (Previously presented): A method of manufacturing a semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, comprising:

a first step of pattern forming said gate above said single crystal semiconductor region through a gate insulating film;

a second step of introducing atoms to amorphize said single crystal semiconductor from oblique directions to a surface of said single crystal semiconductor region with said gate as a mask to form amorphous regions seeping into said single crystal semiconductor region under said gate;

before or after said second step, a third step of introducing impurities into said amorphous regions of said single crystal semiconductor region with said gate as a mask; and

a fourth step of activating said impurities by executing laser irradiation on at least said amorphous regions to form the source and the drain;

wherein an intensity of said laser irradiation is a value of conditions under which said amorphous semiconductor melts but said single semiconductor does not melt.

Claim 2 (Original): The method of manufacturing a semiconductor device according to claim 1, further comprising:

after said fourth step, a fifth step of forming a side wall insulating film on side surfaces of said gate and siliciding surface layers of the source and the drain with said gate and said side wall insulating film as a mask.

Claim 3 (Previously presented): A method of manufacturing a semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, comprising:

a first step of pattern forming said gate above said single crystal semiconductor region through a gate insulating film;

a second step of introducing atoms to amorphize said single crystal semiconductor from oblique directions to a surface of said single crystal semiconductor region with said gate as a mask to form first amorphous regions seeping into said single crystal semiconductor region under said gate;

before or after said second step, a third step of introducing impurities into said first amorphous regions of said single crystal semiconductor region with said gate as a mask to form first junction regions;

a fourth step of forming a side wall insulating film on side surfaces of said gate;

a fifth step of introducing atoms to amorphize said single crystal semiconductor into the surface of said single crystal semiconductor region with said gate and said side wall insulating film as a mask to form second amorphous regions which are deeper than said first amorphous regions;

before or after said fifth step, a sixth step of introducing impurities into said second amorphous regions of said single crystal semiconductor region with said gate and said side wall insulating film as a mask to form second junction regions which are deeper than said first junction regions; and

a seventh step of removing said side wall insulating film and thereafter activating said impurities in said first and second junction regions by executing laser irradiation on at least said amorphous regions to form the source and the drain;

wherein an intensity of said laser irradiation is a value of conditions under which said amorphous semiconductor melts but said single semiconductor does not melt.

Claim 4 (Original): The method of manufacturing a semiconductor device according to claim 3, further comprising:

after said seventh step, an eighth step of forming again a side wall insulating film on the side surfaces of said gate and siliciding surface layers of the source and the drain with said gate and said side wall insulating film as a mask.

Claim 5 (Cancelled)

Claim 6 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein

said gate insulating film is of one type selected from among a silicon oxide film, a silicon nitride film, a silicon oxynitride film and a metal oxide film having a dielectric constant higher than that of the silicon oxide film, or of a film having a laminated structure thereof.

Claim 7 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein

a material of said gate is of one element selected from among silicon, germanium, silicon-germanium and metals.

Claim 8 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein

said atoms to amorphize said single crystal semiconductor are of one element selected from among Si, Ge, As and Ar.

Claim 9 (Previously presented): A method of manufacturing a semiconductor device, comprising the steps of:

introducing atoms to amorphize a single crystal semiconductor using a mask at least twice under different introduction conditions to form each amorphous region having a different depth and area in accordance with each introduction of said atoms;

introducing impurities into said each amorphous region for forming a pn junction before or after each introduction of said atoms; and

activating said introduced impurities by executing laser irradiation on at least said amorphous regions to form said pn junction;

wherein an intensity of said laser irradiation is a value of conditions under which said amorphous semiconductor melts but said single semiconductor does not melt.

Claim 10 (Original): The method of manufacturing a semiconductor device according to claim 9, wherein

at the occasion of the introduction of said atoms, said atoms are introduced from an oblique direction to a surface of said single crystal semiconductor region to seep into said single crystal semiconductor region under said mask at least at one time of introduction of said atoms.

Claim 11 (Cancelled)

Claim 12 (Original): The method of manufacturing a semiconductor device according to claim 9, wherein

said atoms to amorphize said single crystal semiconductor are of one element selected from among Si, Ge, As and Ar.

Claim 13 (Previously presented): A method of manufacturing a semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, comprising:

a first step of pattern forming said gate above said single crystal semiconductor region through a gate insulating film;

a second step of introducing atoms to amorphize said single crystal semiconductor into a surface of said single crystal semiconductor region with said gate as a mask to form amorphous regions;

before or after said second step, a third step of introducing impurities into said amorphous regions of said single crystal semiconductor region with said gate as a mask; and

a fourth step of activating said impurities by executing laser irradiation on at least said amorphous regions to form the source and the drain,

wherein conditions of introducing said atoms in said second step and conditions of intensity of the laser irradiation in said fourth step are controlled respectively to form parts of the source and the drain corresponding to said amorphous regions to seep into said single crystal semiconductor region under said gate; and

wherein the conditions of introducing said atoms are conditions enough for said amorphous regions to seep into said single crystal semiconductor region under said gate, and the conditions of intensity of the laser irradiation are conditions for only said amorphous regions to melt but for said single crystal semiconductor region not to melt .

Claim 14 (Original): The method of manufacturing a semiconductor device according to claim 13, wherein

a capacitance on said source side is 0.25 (fF/μm/side) or more.

Claim 15 (Cancelled)

Claim 16 (Original): The method of manufacturing a semiconductor device according to claim 13, wherein

said atoms to amorphize said single crystal semiconductor are of one element selected from among Si, Ge, As and Ar.

Claim 17 (Original): The method of manufacturing a semiconductor device according to claim 13, wherein

at the occasion of said fourth step, a heat absorbing film is formed on the entire surface and the laser irradiation is performed through said heat absorbing film.

Claim 18 (Previously presented): A method of manufacturing a semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, comprising:

a first step of pattern forming said gate above said single crystal semiconductor region through a gate insulating film;

a second step of forming a side wall insulating film on side surfaces of said gate and introducing impurities to form deep, first junction regions;

a third step of removing said side wall insulating film and thereafter introducing atoms to amorphize said single crystal semiconductor into a surface of said single crystal semiconductor region with said gate as a mask to form amorphous regions;

before or after said second step, a fourth step of introducing impurities into said amorphous regions of said single crystal semiconductor region with said gate as a mask to form shallow, second junction regions; and

a fifth step of activating said impurities in said first and second junction regions by executing laser irradiation on at least said amorphous regions to form the source and the drain,

wherein conditions of introducing said atoms in said third step and conditions of intensity of the laser irradiation in said fifth step are controlled respectively to form parts of the source and the drain corresponding to said amorphous regions to seep into said single crystal semiconductor region under said gate; and

wherein the conditions of introducing said atoms are conditions enough for said amorphous regions to seep into said single crystal semiconductor region under said gate, and the conditions of intensity of the laser irradiation are conditions for only said amorphous regions to melt but for said single crystal semiconductor region not to melt .

Claim 19 (Original): The method of manufacturing a semiconductor device according to claim 18, wherein

a capacitance on said source side is 0.25 (fF/μm/side) or more.

Claim 20 (Cancelled)

Claim 21 (Original): The method of manufacturing a semiconductor device according to claim 18, wherein

said atoms to amorphize said single crystal semiconductor are of one element selected from among Si, Ge, As and Ar.

Claim 22 (Original): The method of manufacturing a semiconductor device according to claim 18, wherein

at the occasion of said fifth step, a heat absorbing film is formed on the entire surface and the laser irradiation is performed through said heat absorbing film.

Claim 23 (Previously presented): A method of manufacturing a semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, comprising:

a first step of pattern forming said gate above said single crystal semiconductor region through a gate insulating film;

a second step of introducing atoms to amorphize said single crystal semiconductor from oblique directions to a surface of said single crystal semiconductor region with said gate as a mask to form amorphous regions seeping into said single crystal semiconductor region under said gate;

before or after said second step, a third step of introducing impurities into said amorphous regions of said single crystal semiconductor region with said gate as a mask; and

a fourth step of activating said impurities by executing laser irradiation on at least said amorphous region to form the source and the drain,

wherein in said second step, tilt angles of the introduction of said atoms with respect to a direction vertical to the surface of said single crystal semiconductor region are controlled to be greater on said source side than on said drain side so as to form said amorphous regions such that an amount of seeping into said single crystal semiconductor region under said gate is greater on said source side than on said drain side; and

a capacitance on said source side is 0.25 (fF/μm/side) or more.

Claim 24 (Cancelled)

Claim 25 (Original): The method of manufacturing a semiconductor device according to claim 23, wherein

said atoms to amorphize said single crystal semiconductor are of one element selected from among Si, Ge, As and Ar.

Claim 26 (Original): The method of manufacturing a semiconductor device according to claim 23, wherein

at the occasion of said fourth step, a heat absorbing film is formed on the entire surface and the laser irradiation is performed through said heat absorbing film.

Claim 27 (Currently amended): A semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, wherein

the source and the drain are constituted by integrating a shallow junction seeping into said single crystal semiconductor under said gate and a deep junction extending under said shallow junction,

at least said shallow junction includes impurities and atoms to amorphize said single crystal semiconductor, and

[[a]] <u>an overlap</u> capacitance between said gate and said source is 0.25 (fF/μm/side) or more.

Claim 28 (Original): The semiconductor device according to claim 27, wherein

said atoms to amorphize said single crystal semiconductor are of one element selected from among Si, Ge, As and Ar.

Claim 29 (Currently amended): A semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, wherein

the source and the drain are constituted by integrating a shallow junction seeping into said single crystal semiconductor under said gate and a deep junction extending under said shallow junction,

at least said shallow junction includes impurities and atoms to amorphize said single crystal semiconductor, and

said shallow junction is formed such that an amount of seeping into said single crystal semiconductor region under said gate is greater on said source side than on said drain side, and [[a]] <u>an overlap</u> capacitance between said gate and said source is 0.25 (fF/μm/side) or more.

Claim 30 (Original): The semiconductor device according to claim 29, wherein

said atoms to amorphize said single crystal semiconductor are of one element selected from among Si, Ge, As and Ar.

Claim 31 (New): The semiconductor device according to claim 27, wherein said overlap capacitance between said gate and said source is a capacitance in a region where said gate electrode and said source overlap one another.

Claim 32 (New): The semiconductor device according to claim 29, wherein said overlap capacitance between said gate and said source is a capacitance in a region where said gate electrode and said source overlap one another.